CLAIMS

1. An integrated circuit, comprising:

a switch;

a capacitor; and

a nonconductive buried diffusion barrier located between said switch and said capacitor, said buried diffusion barrier substantially covering said switch.

2. An integrated circuit as in claim 1 wherein said buried diffusion barrier comprises silicon nitride.

3. An integrated circuit as in claim 1, further comprising a conductive oxygen-diffusion barrier located between said buried diffusion barrier and said capacitor, said capacitor being located on said conductive oxygen-diffusion barrier, wherein said nonconductive buried diffusion barrier and said conductive oxygen-diffusion barrier together continuously cover said switch.

4. An integrated circuit as in claim 1 wherein said conductive oxygen-diffusion barrier comprises titanium aluminum nitride, iridium, and iridium oxide.

5. An integrated circuit as in claim 3, further comprising a nonconductive hydrogen-diffusion barrier layer continuously covering said capacitor and said switch.

6. An integrated circuit as in claim 5 wherein said nonconductive hydrogen-diffusion barrier comprises strontium tantalate.

7. An integrated circuit as in claim 3, further comprising a conductive plug, said conductive plug located between said switch and said conductive oxygen-diffusion barrier, said nonconductive buried diffusion barrier and said conductive oxygen-diffusion barrier together continuously covering said conductive plug.

8. An integrated circuit as in claim 5 wherein said conductive plug comprises tungsten, titanium, and titanium nitride.

9. An integrated circuit as in claim 3, further comprising:

a first insulator layer between said switch and said conductive oxygen-diffusion barrier; and

a second insulator layer located between said first insulator layer and said conductive oxygen-diffusion barrier, said buried diffusion barrier being located

between said first insulator layer and said second insulator layer.

10. An integrated circuit as in claim 9 wherein said buried diffusion barrier is located on said first insulator layer, said second insulator layer is located on at least a portion of said buried diffusion barrier, and said conductive barrier is located at least partially on said second insulator layer.

11. An integrated circuit as in claim 10 wherein said conductive oxygen-diffusion barrier is located on a capacitor portion of said second insulator layer, and wherein said second insulator layer is not present on a switch portion of said buried diffusion barrier.

12. An integrated circuit as in claim 3 wherein said capacitor comprises:

a bottom electrode located on said conductive oxygen-diffusion barrier;

a dielectric thin film located on said bottom electrode;

a top stack-electrode located on said dielectric thin film; and

a top plate-line electrode, a portion of said top plate-line electrode being located on said top stack-electrode, said top plate-line electrode defining a plate-line axis;

wherein said conductive oxygen-diffusion barrier, said bottom electrode, said dielectric thin film, and said top stack-electrode are included in a self-aligned capacitor stack located on a capacitor portion of said second insulator layer.

13. An integrated circuit as in claim 12 wherein said capacitor stack has an insulated sidewall substantially perpendicular to said plate-line axis, and wherein said capacitor stack has a protected sidewall substantially parallel to said plate-line axis.

14. An integrated circuit as in claim 13, further comprising:

a third insulator layer;

wherein said insulated sidewall comprises an edge of said conductive barrier, an edge of said bottom electrode, and an edge of said dielectric thin film, and wherein a portion of said third insulator layer covers said insulated sidewall.

15. An integrated circuit as in claim 13 wherein said protected sidewall comprises an edge of said second insulator layer, an edge of said conductive oxygen-diffusion barrier, an edge of said bottom electrode, an edge of said dielectric thin film, and an edge of said top plate-line electrode.

16. An integrated circuit as in claim 13, further comprising:

a nonconductive hydrogen-diffusion barrier layer that continuously covers said capacitor and said switch;

wherein said nonconductive hydrogen-diffusion barrier comprises a plate-line portion covering said plate-line, a sidewall portion covering said protected sidewall, and a switch-portion located on a switch portion of said buried diffusion barrier.

17. An integrated circuit as in claim 16 wherein said nonconductive hydrogen-diffusion barrier does not cover a nonmemory area of said integrated circuit.

18. An integrated circuit as in claim 16 wherein said nonconductive hydrogen-diffusion barrier comprises strontium tantalate.

19. An integrated circuit as in claim 18 wherein said nonconductive hydrogen-diffusion barrier further comprises silicon nitride.

20. An integrated circuit as in claim 12 wherein said top plate-line electrode is wider than the capacitor stack in an orientation parallel to said plate-line axis.

21. An integrated circuit as in claim 12, further comprising a plate-line connector located remotely from said capacitor stack.

22. An integrated circuit as in claim 12, further comprising a bit-line plug, said bit-line plug comprising a bottom end and a top end, said bottom end in electrical contact with said switch, and said top end in electrical contact with a wiring layer.

23. An integrated circuit as in claim 22 wherein said bit-line plug comprises tungsten.

24. An integrated circuit as in claim 12 wherein said dielectric thin film comprises a ferroelectric layered superlattice material.

25. An integrated circuit as in claim 24 wherein said thin film comprises ferroelectric layered superlattice material selected from the group consisting of strontium bismuth tantalate and strontium bismuth tantalum niobate.

26. An integrated circuit as in claim 24 wherein said thin film has a thickness not exceeding 90 nm.

27. An integrated circuit as in claim 1, further comprising a plurality of switches, said electrically nonconductive buried diffusion barrier continuously covering said plurality of switches.

28. An integrated circuit comprising:

a first oxide insulation layer disposed on an extended surface area of a substrate; and

a nonconductive buried diffusion barrier layer located on said first insulation layer, said buried diffusion barrier layer continuously covering said extended surface area.

29. An integrated circuit as in claim 28, further comprising a second oxide insulation layer above said first oxide insulation layer, said buried diffusion barrier layer located between said first insulation layer and said second insulation layer.

30. An integrated circuit as in claim 28, further comprising:

a second diffusion barrier proximate to said buried diffusion barrier;

a first integrated circuit element below said buried diffusion barrier; and

a second integrated circuit element above said buried diffusion barrier and above said second diffusion barrier;

wherein said buried diffusion barrier and said second diffusion barrier form a continuous diffusion barrier separating said first integrated circuit element from said second integrated circuit element.

31. An integrated circuit as in claim 30 wherein said second diffusion barrier layer comprises titanium nitride.

32. An integrated circuit as in claim 28 wherein said buried diffusion barrier layer comprises silicon nitride.

33. An integrated circuit, comprising:

a switch;

a capacitor comprising a top plate-line electrode;

a conductive plug between said switch and said capacitor;

a conductive oxygen-diffusion barrier located separating said switch and said plug from said capacitor, said capacitor being located on said conductive oxygen-diffusion barrier; and

a nonconductive hydrogen-diffusion barrier layer continuously covering said capacitor and said switch.

34. An integrated circuit as in claim 33 wherein said conductive oxygen-diffusion barrier comprises titanium aluminum nitride, iridium, and iridium oxide.

35. An integrated circuit as in claim 33 wherein said nonconductive hydrogen-diffusion barrier comprises strontium tantalate.

36. An integrated circuit as in claim 33 wherein said nonconductive hydrogen-diffusion barrier layer and said conductive oxygen-diffusion barrier together form a continuous diffusion barrier layer separating said capacitor from said switch and said conductive plug.

37. An integrated circuit as in claim 33 wherein said capacitor comprises a top plate-electrode, a dielectric thin film, and a bottom electrode located on said conductive oxygen-diffusion barrier, and wherein said nonconductive hydrogen-diffusion barrier layer and said conductive oxygen-diffusion barrier continuously envelop said capacitor.

38. An integrated circuit as in claim 33, further comprising:

a first insulator layer between said switch and said conductive oxygen-diffusion barrier; and

a third insulator layer, a switch portion of said third insulator being located on a switch area of said integrated circuit, and a residual portion of said third insulator layer being located on a sidewall of said capacitor.

39. An integrated circuit as in claim 38 wherein said nonconductive hydrogen barrier layer is located on said top plate-electrode, on said residual portion on said sidewall of said capacitor, and on said switch portion of said third insulator.

40. An integrated circuit as in claim 33 wherein said nonconductive hydrogen-diffusion barrier does not cover a nonmemory area of said integrated circuit.

41. An integrated circuit as in claim 33 wherein:

said capacitor comprises a self-aligned capacitor stack comprising a top stack-electrode, a dielectric thin film, a bottom electrode, and said conductive oxygen-diffusion barrier; and

wherein said top plate-line electrode defines a plate-line axis, and said top plate-line electrode is wider than said capacitor stack in an orientation parallel to said plate-line axis.

42. An integrated circuit as in claim 33, further comprising an electrical connector to said top plate-line electrode, said electrical connector located remotely from said capacitor stack.

43. A method of fabricating an integrated circuit, comprising:

providing a substrate, said substrate comprising a switch and a first insulator layer covering said switch;

forming a nonconductive buried diffusion barrier layer on said first insulator layer; and

forming a second insulator layer on said nonconductive buried diffusion barrier layer.

44. A method as in claim 43, further comprising:

forming a conductive plug with a bottom end and a top end, said bottom end in electrical contact with said switch;

planarizing said top end and said second insulator layer;

forming a conductive oxygen-diffusion barrier layer on said second insulator layer and on said top end of said conductive plug;

forming a bottom electrode layer on said conductive oxygen-diffusion barrier layer;

forming a dielectric thin film on said bottom electrode layer;

forming a top stack-electrode layer on said dielectric thin film; and

removing portions of said top stack-electrode layer, said dielectric thin film, said bottom electrode layer, and said conductive oxygen-diffusion barrier layer, thereby forming a capacitor stack comprising a top stack-electrode, a dielectric thin film, a bottom electrode, and a conductive oxygen-diffusion barrier, said conductive oxygen-diffusion barrier being in electrical contact with said top end of said conductive plug, said capacitor stack comprising a stack sidewall, and said top stack-electrode having a top surface.

45. A method as in claim 44, further comprising:

forming a third insulator layer on said substrate, thereby depositing a portion

of said third insulator layer on said stack sidewall and on said second insulator layer;

removing a portion of said third insulator layer completely from at least a contact portion of said top surface of said top stack-electrode;

thereafter forming a top plate-line electrode layer on said contact portion of said top stack-electrode and on said third insulator layer;

removing a portion of said top plate-line electrode layer from a switch area of said substrate;

removing a portion of said third insulator layer from said switch area of said substrate; and

removing a portion of said second insulator layer from said switch area of said substrate;

thereby exposing an exposed portion of said buried diffusion barrier layer on a bit-line side of said capacitor stack, and further thereby forming a protected sidewall, said protected sidewall comprising a plate-line edge, top stack-electrode edge, a dielectric thin film edge, a bottom electrode edge, a conductive oxygen-diffusion barrier edge, and a second insulator layer edge.

46. A method as in claim 45, further comprising forming a nonconductive hydrogen-diffusion barrier layer on said top plate-line electrode, on said protected sidewall, and on said exposed portion of said buried diffusion barrier layer.

47. A method as in claim 45, further comprising removing a portion of said nonconductive hydrogen barrier layer from a nonmemory area of said substrate.

48. A method as in claim 45, further comprising:

forming a fourth insulator layer on said substrate;

forming an electrical connection to said top plate-line electrode remotely from said capacitor stack; and

forming an electrical connection to said switch.

49. A method of fabricating an integrated circuit, comprising:

providing a substrate, said substrate comprising a switch and a capacitor stack, said capacitor stack comprising a top stack-electrode, a thin film of capacitor dielectric, a bottom electrode, and a conductive oxygen-diffusion barrier, said

conductive oxygen-diffusion barrier located above said switch;

forming a top plate-line electrode on said top stack-electrode; and

forming a continuous electrically nonconductive hydrogen-diffusion barrier layer on said plate-line electrode, on a protected side of said capacitor stack, and on a switch area of said substrate.

50. A method of fabricating a ferroelectric integrated circuit, comprising:

providing a substrate including a switch and a first insulator layer covering said switch;

forming a conductive plug through said first insulator layer, said conductive plug having a bottom end and a top end, said bottom end in electrical contact with said switch;

planarizing said top end of said conductive plug;

forming a stack of capacitor layers over said conductive plug, said stack including a bottom electrode layer, a thin film capacitor ferroelectric layer, and a top stack-electrode layer;

removing portions of said top stack-electrode layer, said ferroelectric thin film, and said bottom electrode layer, thereby forming a plurality of separated capacitor stacks, each comprising a top stack-electrode, a ferroelectric thin film, and a bottom electrode;

forming a capacitor insulator layer over said capacitor stacks, filling in said removed portions and thereby insulating said capacitor stacks from one another and protecting their sides;

removing a portion of said capacitor insulator layer from at least a contact portion of said top surface of said top stack-electrodes; and

thereafter forming a top plate-line electrode layer on said contact portion of said top stack-electrode and on said capacitor insulator layer.

51. A method as in claim 50 wherein said forming a stack of capacitor layers further comprises forming a conductive oxygen-diffusion barrier layer prior to forming said bottom electrode layer, and said removing portions of said top stack-electrode layer includes removing portions of said conductive oxygen-diffusion barrier layer.

52. A method as in claim 51 wherein said removing portions of said top

stack-electrode layer comprises:

depositing a hardmask on said top stack-electrode;

patterning said hardmask;

etching said top stack-electrode layer, said ferroelectric thin film, and said bottom electrode layer;

removing said hard mask; and

etching said barrier layer.

53. A method as in claim 50 wherein said top-stack electrode layer is from 5 nm to 100 nm thick.

54. A method as in claim 53 wherein said top-stack electrode layer is 50 nm thick.

55. A method as in claim 50 wherein said removing portions of said top stack-electrode layer comprises:

depositing a hardmask on said top stack-electrode;

patterning said hardmask;

etching said top stack-electrode layer, said ferroelectric thin film, and said bottom electrode layer; and

removing said hard mask.

56. A method as in claim 50 wherein removing a portion of said capacitor insulator layer comprises planarizing said capacitor insulator layer to expose said top stack-electrodes.

57. A method as in claim 50, and further comprising crystallizing said ferroelectric layer prior to said removing portions of said top stack-electrode layer, said ferroelectric thin film, and said bottom electrode layer.

58. A method as in claim 50, and further comprising crystallizing said ferroelectric layer after said removing portions of said top stack-electrode layer, said ferroelectric thin film, and said bottom electrode layer.

59. A method as in claim 50 wherein said forming a stack of capacitor layers comprises using a low-thermal-budget technique to form a thin film of ferroelectric layer superlattice material having a thickness less than 100 nm, and heating said substrate at an elevated temperature exceeding 500°C for a cumulative heating time of less than five minutes.

60. An integrated circuit, comprising:

a switch;

a capacitor;

a conductive plug disposed between said switch and said capacitor;

a conductive oxygen-diffusion barrier between said conductive plug and said capacitor; and

a nonconductive buried diffusion barrier located between said switch and said capacitor, said conductive oxygen-diffusion barrier and said nonconductive buried diffusion barrier forming a continuous diffusion barrier separating said capacitor from said switch and said conductive plug.

61. An integrated circuit, comprising:

a switch;

a capacitor;

a conductive plug disposed between said switch and said capacitor;

a conductive oxygen-diffusion barrier between said conductive plug and said capacitor; and

a nonconductive hydrogen-diffusion barrier layer continuously covering said capacitor and said switch;

wherein said nonconductive hydrogen-diffusion barrier layer and said conductive oxygen-diffusion barrier together form a continuous diffusion barrier layer separating said capacitor from said switch and said conductive plug.

62. An integrated circuit, comprising:

a switch;

a capacitor;

a conductive plug disposed between said switch and said capacitor;

a conductive oxygen-diffusion barrier between said conductive plug and said capacitor; and

a nonconductive hydrogen-diffusion barrier layer continuously covering said capacitor and said switch;

wherein said nonconductive hydrogen-diffusion barrier layer covers a protected side of said capacitor.

63. An integrated circuit as in claim 62 wherein said nonconductive

hydrogen-diffusion barrier layer comprises strontium tantalate.

64. An integrated circuit as in claim 62 wherein said capacitor comprises a top electrode, a dielectric thin film, and a bottom electrode, and said nonconductive hydrogen-diffusion barrier layer covers a top electrode edge, a dielectric thin film edge, and a bottom electrode edge at said protected side.

65. An integrated circuit as in claim 64 further comprising a conductive oxygen-barrier disposed below said bottom electrode, and wherein said nonconductive hydrogen-diffusion barrier layer covers a conductive oxygen-barrier edge at said protected side.

66. An integrated circuit as in claim 64, further comprising an insulator layer disposed below said conductive oxygen-barrier between said switch and said conductive oxygen-barrier, and wherein said nonconductive hydrogen-diffusion barrier layer covers an insulator layer edge at said protected side.